



INTERNATIONAL WORKSHOP ON APPLIED
RECONFIGURABLE COMPUTING (ARC2006)
DELFT, THE NETHERLANDS, MARCH 1-3, 2006

List of the Accepted Papers

Applications

Andre Guntoro^o, Peter Zipf^o, Oliver Soffke^o, Harald Klingbeil², Martin Kumm², Manfred Glesner^o, ^oInstitute of Microelectronic Systems, Darmstadt University of Technology, Germany; ²Gesellschaft für Schwerionenforschung mbH, Darmstadt, Germany, ***Implementation of Realtime and Highspeed Phase Detector on FPGA***

Gerd Van den Branden^{o2}, Geert Braeckman^o, Abdellah Touhafi^{o2}, Erik Dirckx², ^oErasmushogeschool Brussel, Dept. IWT, Brussel, Belgium; ²Vrije Universiteit Brussel (VUB), Brussels, Belgium, Case Study: ***Implementation of a Virtual Instrument on a Dynamically Reconfigurable Platform***

Rodrigo Piedade, Leonel Sousa, Electrical and Computer Eng. Dept., IST/INESC – ID; Portugal, ***Configurable Embedded Core for Controlling Electro-Mechanical Systems***

Power

K. Heyrman^o, A. Papanikolaou², F. Catthoorⁿ, P. Veelaert^o, K. Debosschere^{oo}, W. Philips²², ^oHogeschool Gent, Belgium; ²IMEC, Belgium; ⁿIMEC and Katholieke Universiteit Leuven, Belgium; ^{oo}ELIS, Ghent University, Belgium; ²²TELIN, Ghent University, Belgium, ***Energy Consumption for Transport of Control Information on a Segmented Software-Controlled Communication Architecture***

H. Joshi^o, S.S. Verma², G. K. Sharmaⁿ, ^oM.L.V. Textile and Engineering College, Bhilwara, India; ²Flextronics Software Systems, Gurgaon India; ⁿABV-Indian Institute of Information Technology and Management, Gwalior, India, ***Quality Driven Dynamic Low Power Reconfiguration of Handhelds***

K. Siozios, S. Mamagkakis, D. Soudris, A. Thanailakis, VLSI Design and Testing Center, Dept. of Electrical and Computer Engineering, Democritus University of Thrace, Xanthi, Greece, ***Designing Heterogeneous FPGAs with Multiple SBs***

Image processing

Javier Díaz^o, Eduardo Ros^o, Sonia Mota², Rafael Rodriguez-Gomez^o, ^oDep. Arquitectura y Tecnología de Computadoras, Universidad de Granada, Spain; ²Dep. Informática y Análisis Numérico, Universidad de Córdoba, Spain, ***Highly Parallelized Architecture for Image Motion Estimation***

Niklas Lepistö, Benny Thörnberg, Mattias O'Nils, Mid Sweden University – Dept. Information Technology and Media, Sweden, ***Design Exploration of a Video Pre-Processor for an FPGA based SoC***

Sunil Shukla^{o2}, Neil Bergmann^o, Jürgen Becker², ^oITEE University of Queensland - Brisbane QLD, Australia; ²ITIV, Universität Karlsruhe, Germany, ***QUKU: A Fast Run Time Reconfigurable Platform for Image Edge Detection***

Kevin Dale^o, Jeremy Sheaffer^o, Vinu Kumar², David Luebke^o, Greg Humphreys^o, Kevin Skadron^o, ^oDept. of Computer Science, ²Dept. of Electrical and Computer Engineering, University of Virginia, USA, ***Applications of Small-Scale Reconfigurability to Graphics Processors***



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Vanderlei Bonato, José de Hollanda, Eduardo Marques, Institute of Mathematics and Computing Sciences, University of Sao Paulo, Brazil, ***An Embedded Multi-Camera System for Simultaneous Localization and Mapping***

Vu Manh Tuan, Y. Hasegawa, N. Katsura, H. Amano, Graduate school of Science and Techn., Keio University – Tokyo; Japan, ***Performance/Cost trade-off evaluation for the DCT implementation on the Dynamically Reconfigurable Processor***

Francisco Fons^o, Mariano Fons^o, Enrique Cantó^o, Mariano López², ^oDep. D'Enginyeria Electrònica, Elèctrica I Automàtica, Universitat Rovira i Virgili ETSE, Tarragona, Spain; ²Dep.d'Enginyeria Electrònica, Universitat Politècnica de Catalunya, EPSEVG, Spain, ***Trigonometric Computing Embedded in a Dynamically Reconfigurable CORDIC System-on-Chip***

Slawomir Cichón, Marek Gorgoń, Miroslaw Pac, AGH University of Science and Technology, Biocybernetic Lab, Dept. of Automatics, Kraków, Poland, ***Handel-C design enhancement for FPGA- based DV Decoder***

Alex Nguouanga^o, Andre Borin Suarez², Gilles Sassatelli^o, Lionel Torres^o, ^oUniversité Montpellier II-LIRMM, France; ²Universidade Federal do Rio Grande do Sul (UFRGS), Brazil, ***Run-time resources management on coarse grained, packet switching reconfigurable architectures: a case study through aPACHES platform***

Young-Ho Seo^o, Dong-Wook Kim², ^oDept. of Information and Communication Eng., Hansung University, Seoul, Korea; ²Dept. Of Electronic Materials Engineering, Kwangwoon University, Seoul, Korea, ***A New VLSI Architecture of Lifting-based DWT***

Organization and Architecture

Hui Qin^o, Tsutomu Sasao^o, Jon. Butler², ^oDept. of Computer Science and Electronics, Kyushu Institute of Technology, Japan; ²Dept. Of Electrical and Computer Engineering, Naval Postgraduate School, Monterey, CA, USA, ***Implementation of LPM Address Generator on FPGAs***

Rainer Scholz, Klaus Buchenrieder, Universität der Bundeswehr München, Germany, ***Self Reconfiguring EPIC Soft Core Processors***

S. Román, J. Septién, H. Mecha, D. Mozos, Dep. de Arquitectura de Computadores y Automática, Universidad Complutense, Madrid, Spain, ***Constant complexity management of 2D HW multitasking in Run-Time Reconfigurable FPGAs***

Mário Véstias^o, Horácio C. Neto², ^oISEL/INESC-ID; Portugal; ²INESC-ID, Portugal, ***Area/Performance Improvement of NoC Architectures***

Kwang-sup So, Jinsang Kim, Won-Kyung Cho, Young-Soo Kim, Doug Young Suh, School of Electronics and Information - Kyung Hee University; Korea, ***Implementation of Inner Product Architecture for Increased Flexibility in Bitwidths of Input Array***

Su Shin Ang^o, George Constandinides^o, Peter Cheung^o, Wayne Luk², ^oDept. of Electrical and Electronics Engineering, Imperial College, London; ²Dept. Of Computing , Imperial College, London, ***A Flexible Multi-Port Caching Scheme for Reconfigurable Platforms***



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Nikos Vassiliadis, George Theodoridis, Spiridon Nikolaidis, Section of Electronics and Computers, Physics Department - Aristotle University of Thessaloniki; Greece, ***Enhancing a Reconfigurable Instruction Set Processor with Partial Predication and Virtual Opcode Support***

D. Benitez^o, J.C. Moure², D.I. Rexachs², E. Luque², ^oIUSIANI and DIS Dept. University of Las Palmas G.C., Las Palmas, Spain; ²Computer Architecture and Operating System Dept. Universitat Autònoma Barcelona, Spain, ***A Reconfigurable Data Cache for Adaptive Processors***

Daniel Poznanovic, SRC Computers Inc., Colorado Springs, CO, USA, ***The emergence of non-von Neumann processors***

Marcelo Götzt, Florian Dittmann, Heinz Nixdorf Institute - University of Paderbronn, Germany, ***Scheduling Reconfiguration Activities of Run-time Reconfigurable RTOS Using an Aperiodic Task Server***

Manuel Gericota^o, Gustavo Alves^o, Luís Lemos^o, José Ferreira², ^oDept. of Electrical Engineering -ISEP, Porto Portugal; ²Dept. of Electrical and Computer Eng. - FEUP, Porto, Portugal, ***A New Approach to Assess Defragmentation Strategies in Dynamically Reconfigurable FPGAs***

Minoru Watanabe, Fuminori Kobayashi, Dept.of Systems Innovation and Informatics, Kyushu Institute of Technology, Japan, ***A 1,632 gate-count zero-overhead Dynamic Optically Reconfigurable Gate Array VLSI***

Networks and Communication

Sanjay P Singh, S. Bhoj, D. Balasubramanian, T. Nagda, D. Bhatia, P. Balsara, Center for Integrated Circuits and Systems; University of Texas, USA, ***Generic Network Interface for Plug and Play NoC based Architecture***

Nikolay Kavaldjiev, Gerard Smit, Pascal Wolkotte, P. Jansen, Faculty of Electrical Engineering, Mathematics and Computer Science, University of Twente, the Netherlands, ***Providing QoS Guarantees in a NoC by Virtual Channel Reservation***

Milan Tichy^o, Jan Schier², David Gregg^o, ^oUniversity of Dublin, Trinity College, Dept. of Computer Science, Dublin, Ireland; ²Institute of Information Theory and Automation, Academy of Sciences of the Czech Rep., Czech Republic, ***Efficient Floating-Point Implementation of High-Order (N)LMS Adaptive Filters in FPGA***

HongzhiWang, Pierre Leray, Jacques Palicot, IETR/ Supelec – Campus de Rennes, France, ***A reconfigurable architecture for MIMO Square Root Decoder***

Security

Nele Mentens, L. Batina, B. Preneel, I. Verbauwhede, Katholieke Universiteit Leuven, ESAT/SCD-COSIC; Belgium, ***Time-memory trade-off attack on FPGA platforms: UNIX password cracking***

F.-X. Standaert, F. Mace, E. Peeters, J.-J. Quisquater, UCL Crypto Group; Belgium, ***Updates on the Security of FPGAs against Power Analysis Attacks***



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K. Sakiyama, N. Mentens, L. Batina, B. Preneel, I. Verbauwhede, Katholieke Universiteit Leuven, ESAT/COSIC; Belgium, **Reconfigurable Modular Arithmetic Logic Unit for High-performance Public-key Cryptosystems**

Maurice Keller, Tim Kerins, Francis Crowe, William Marnane, Dept. of Electrical and Electronic Engineering, University College Cork; Ireland, **FPGA Implementation of a $GF(2^m)$ Tate Pairing Architecture**

Guerric Meurice de Dormale, Jean-Jacques Quisquater, Université Catholique de Louvain, UCL, Crypto Group, DICE; Belgium, **Iterative Modular Division over $GF(2^m)$: Novel Algorithm and Implementations on FPGA**

David Rodríguez, Juan M. Sánchez, Arturo Durán, Area de Arquitectura y Tecnología de los Computadores Escuela Politécnica, Universidad de Extremadura; Spain, **Mobile Fingerprint Identification using a Hardware Accelerated Biometric Service Provider**

S. Yusuf, W. Luk, M. Szeto, W. Osborne, Dept. of Computing, Imperial College London, UK, **UNITE: uniform hardware-based network intrusion detection engine**

Tools

Betul Buyukkurt, Zhi Guo, Walid Najjar, Dept. of Computer Science and Engineering, University of California-Riverside; USA, **Impact of Loop Unrolling on Area, Throughput and Clock Frequency in ROCCC: C to VHDL Compiler for FPGAs**

Dinesh Suresh, Zhi Guo*, Betul Buyukkurt, Walid Najjar, Dept. of Computer Science and Engineering; *Dept. of Electrical Engineering, University of California-Riverside; USA, **Automatic compilation framework for Bloom filter based intrusion detection**

Jie Guo^o, Gleb Belov², Gerhard Fettweis^o, ^oVodafone Chair Mobile Communication Systems – TU Dresden, Germany; ²Fak. Mathematics and Natural Sciences, T.U. Dresden, Germany, **A Basic Data Routing Model for a Coarse-grain Reconfigurable Hardware**

B. De Sutter^o, B. Mei^o, A. Bartic^o, T. Vander Aa^o, M. Berekovic^o, J-Y Mignolet^o, K. Croes^o, P. Coene^o, M. Cupac^o, A. Couvreur^o, A. Folens^o, S. Dupont^o, B. Van Thienen^o, A. Kanstein², H-S. Kimⁿ, S.J. Kimⁿ, ^oIMEC; Belgium; ²Freescale Semiconducteurs France SAS, France; ⁿSamsung Advanced Inst. of Techn., **Hardware and tool chain implementation for a coarse-grained reconfigurable architecture**

Jack Whitham, Neil Audsley, Dept. of Computer Science, University of York, York, UK, **Integrating Custom Instruction Specifications into C Development Processes**

Jens Braunes, Rainer G. Spallek, Institute of Computer Engineering, Technische Universität Dresden; Germany, **A Compiler-Oriented Architecture Description for Reconfigurable Systems**

Antonio Beck, Victor Gomes, Luigi Carro, Instituto de Informática – Universidade Federal do Rio Grande do Sul, Brazil, **Dynamic Instruction Merging and a Reconfigurable Array: Dataflow Execution with Software Compatibility**

Jae-Jin Lee, Gi-Yong Song, School of Electrical and Computer Eng., Chungbuk National University; Korea, **High-Level Synthesis Using SPARK and Systolic Array**



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Posters

J. Gonzalez-Gomez, I. Gonzales, F. Gomez-Arribas, E. Boemo, Universidad Autonoma de Madrid, Spain, ***Evaluation of a locomotion algorithm for worm-like robots on FPGA-embedded processors***

Ignacio Bravo, Pedro Jimenez, Manuel Mazo, Jose Luis Lazaro, Ernesto Martin, Electronics dept. University of Alcalá, Spain, ***Architecture based on FPGA's for real-time image processing***

Yeong-Jae Oh, Hanho Lee, Chong-Ho Lee, School of Information and Communication Engineering, Inha University, Korea, ***Dynamic Partial Reconfigurable FIR Filter Design***

Rodrigo Agis, Javier Diaz, Eduardo Ros, Richard Carillo, Eva Ortigosa, University of Granada, Spain, ***Event-driven simulation engine for spiking neural networks on a chip***

Eva Ortigosa, A. Canas, R. Rodriguez, J. Diaz, S. Mota, University of Granada, Spain, ***Towards an optimal implementation of MLP in FPGA***

E. Ros, J. Diaz, F. Vargas-Martin, M.D. Pelaez-Coca, University of Granada, Spain, ***Real time image processing on a portable aid device for low vision patients.***

S. Mota, E. Ros, J. Diaz, F. de Toro, University of Cordoba, University of Granada, Spain, ***General purpose real-time image segmentation system***

Joon ho park, Bang-Hyun Sung, Seok-Yoon Kim, Soongsil University, Korea, ***An Efficient Estimation Method of Dynamic Power Dissipation on VLSI Interconnects***

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