2006 APPLIED RECONFIGURABLE COMPUTING WORKSHOP

WEDNESDAY MARCH 1, 2006

	APPLICATIONS	**SESSION CHAIR : K. BERTELS**	
09:30	George Constantinides (invited talk)	Imperial College, UK	Efficient and Automated Fixed-Point Implementation
10:20	Andre Guntoro°, Peter Zipf°, Oliver Soffke°, Harald Klingbeil², Martin Kumm², Manfred Glesner°	°Institute of Microelectronis Systems, Darmstadt University of Technology, Germany; ²Gesellschaft für Schwerionenforschung mbH, Darmstadt, Germany	Implementation of Realtime and Highspeed Phase Detector on FPGA
10:45	Gerd Van den Branden°², Geert Braeckman°, Abdellah Touhafi°², Erik Dirkx²	°Erasmushogeschool Brussel, Dept. IWT, Brussel, Belgium; ²Vrije Universiteit Brussel (VUB), Brussels, Belgium	Case Study: Implementation of a Virtual Instrument on a Dynamically Reconfigurable Platform
11:00	Rodrigo Piedade, Leonel Sousa	Electrical and Computer Eng. Dept., IST/INESC – ID; Portugal	Configurable Embedded Core for Controlling Electro-Mechanical Systems
11:15	**BREAK**		**POSTER**
11:35	**POWER**	**SESSION CHAIR : GEORGE CONSTANTINIDES**	
11:35	K. Heyrman°, A. Papanikolaou², F. Catthoorⁿ, P. Veelaert°, K. Debosschere°°, W. Philips²²	°Hogeschool Gent, Belgium; ²IMEC, Belgium; ⁿIMEC and Katholieke Universiteit Leuven, Belgium; °°ELIS, Ghent University, Belgium; ²²TELIN, Ghent University, Belgium	Energy Consumption for Transport of Control Information on a Segmented Software-Controlled Communication Architecture
11:50	H. Joshi°, S.S. Verma², G. K. Sharmaⁿ	°M.L.V. Textile and Engineering College, Bhilwara, India; ²Flextronics Software Systems, Gurgaon India; ⁿABV-Indian Institute of Information Technology and Management, Gwalior, India	Quality Driven Dynamic Low Power Reconfiguration of Handhelds
12:05	K. Siozios, S. Mamagkakis, D. Soudris, A. Thanailakis	VLSI Design and Testing Center, Dept. of Electrical and Computer Engineering, Democritus University of Thrace, Xanthi, Greece	Designing Heterogeneous FPGAs with Multiple SBs
12:20	**LUNCH**		
13:40	**IMAGE PROCESSING**	**SESSION CHAIR : JOAO CARDOSO**	
13:40	Javier Díaz°, Eduardo Ros°, Sonia Mota², Rafael Rodrigez-Gomez°	°Dep. Arquitectura y Tecnología de Computadoras, Universidad de Granada, Spain; ²Dep. Infórmatica y Análisis Numérico, Univeridad de Córdoba, Spain	Hihgly Parallellized Architecture for Image Motion Estimation
14:05	Niklas Lepistö, Benny Thörnberg, Mattias O'Nils	Mid Sweden University – Dept. Information Technology and Media, Sweden	Design Exploration of a Video Pre-Processor for an FPGA based SoC
14:20	Sunil Shukla°²,Neil Bergmann°, Jürgen Becker²	°ITEE University of Queensland - Brisbane QLD, Australia; ²ITIV, Universität Karlsruhe, Germany	QUKU: A Fast Run Time Reconfigurable Platform for Image Edge Detection
14:35	Kevin Dale°, Jeremy Sheaffer°, Vinu Kumar², David Luebke°, Greg Humphreys°, Kevin Skadron°	°Dept. of Computer Science, ²Dept. of Electrical and Computer Engineering, University of Virginia, USA	Applications of Small-Scale Reconfigurability to Graphics Processors
15:00	Vanderlei Bonato, José de Hollanda, Eduardo Marques	Institute of Mathematics and Computing Sciences, University of Sao Paulo, Brazil	An Embedded Multi-Camera System for Simultaneous Localization and Mapping
15:15	Vu Manh Tuan, Y. Hasegawa, N. Katsura, H. Amano	Graduate school of Science and Techn., Keio University – Tokyo; Japan	Performance/Cost trade-off evaluation for the DCT implementation on the Dynamically Reconfigurable Processor
15:30	**BREAK**		**POSTER**
15:50	Francisco Fons°, Mariano Fons°, Enrique Cantó°, Mariano López²	°Dep. D'Enginyeria Electrònica, Elèctrica I Automàtica, Universitat Rovira i Virgili ETSE, Tarragona, Spain; ²Dep.d'Enginyeria Electrònica, Universitat Politècnica de Catalu;nya, EPSEVG, Spain	Trigonometric Computing Embedded in a Dynamically Reconfigurable CORDIC System-on-Chip
16:05	Slawomir Cichón, Marek Gorgoń, Miroslaw Pac	AGH University of Science and Technology, Biocybernetic Lab, Dept. of Automatics, Kraków, Poland	Handel-c design enhancement for FPGA- based DV Decoder

16:20	Alex Ngouanga°, Andre Borin Suarez², Gilles Sassatelli°, Lionel Torres°	°Université Montpellier II-LIRMM, France; ²Universidad Federal do Rio Grande do Sul (UFRGS), Brazil	Run-time resources management on coarse grained, packet switching reconfigurable architectures: a case study through aPACHES platform
16:45	Young-Ho Seo°, Dong-Wook Kim²	°Dept. of Inforamation and Communication Eng., Hansung University, Seoul, Korea; ²Dept. Of Electronic Materials Engineering, Kwangwoon University, Seoul, Korea	A New VLSI Architecture of Lifting-based DWT
17:00	**BREAK**		**POSTER**
17:15	**ORGANISATION AND ARCHITECTURE**	**SESSION CHAIR : MLADEN BEREKOVIC**	
17:25	Hui Qin°, Tsutomu Sasao°, Jon. Butler²	°Dept. of Computer Science and Electronics, Kyushu Institute of Technology, Japan; ²Dept. Of Electrical and Computer Engineering, Naval Postgraduate School, Monterey, CA, USA	Implementation of LPM Address Generator on FPGAs
17:50	Rainer Scholz, Klaus Buchenrieder	Universität der Bundeswehr München, Germany	Self Reconfiguring EPIC Soft Core Processors
18:05	S. Román, J. Septién, H. Mecha, D. Mozos	Dep. de Arquitectura de Computadores y Automática, Universidad Complutense, Madrid, Spain	Constant complexity management of 2D HW multitasking in Run-Time Reconfigurable FPGAs
18:20	**RECEPTION AT THE COMPUTER ENGINEERING LAB (1st floor)**	**PANEL DISCUSSION**	

THURSDAY MARCH 1, 2006

	ORGANISATION AND ARCHITECTURE	**SESSION CHAIR : MLADEN BEREKOVIC**	
09:00	Stamatis Vassiliadis (invited talk)	Delft University of Technology, the Nethelands	Polymorphic Instruction Set Computers
09:40	Mário Véstias°, Horácio C. Neto²	°ISEL/INESC-ID; Portugal; ²INESC-ID, Portugal	Area/Performance Improvement of NoC Architectures
09:55	Kwang-sup So, Jinsang Kim, Won-Kyung Cho, Young-Soo Kim, Doug Young Suh	School of Electronics and Information - Kyung Hee University; Korea	Implementation of Inner Product Architecture for Increased Flexibility in Bitwidths of Input Array
10:10	Su Shin Ang°, George Constandinides°, Peter Cheung°, Wayne Luk²	°Dept. of Electrical and Electronics Engineering, Imperial College, London; ²Dept. Of Computing , Imperial College, London	A Flexible Multi-Port Caching Scheme for Reconfigurable Platforms
10:35	Nikos Vassiliadis, George Theodoridis, Spiridon Nikolaidis	Section of Electronics and Computers, Physics Department - Aristotle University of Thessaloniki; Greece	Enhancing a Reconfigurable Instruction Set Processor with Partial Predication and Virtual Opcode Support
11:00	**BREAK**		**POSTER**
11:20	D. Benitez°, J.C. Moure², D.I. Rexachs², E. Luque²	°IUSIANI and DIS Dept. University of Las Palmas G.C., Las Palmas, Spain; ²Computer Architecture and Operating System Dept. Universitat Autonoma Barcelona, Spain	A Reconfigurable Data Cache for Adaptive Processors
11:45	Daniel Poznanovic	SRC Computers Inc., Colorado Springs, CO, USA	The emergence of non-von neumann processors
12:10	Marcelo Götz, Florian Dittmann	Heinz Nixdorf Institute - University of Paderbron, Germany	Scheduling Reconfiguration Activities of Run-time Reconfigurable RTOS Using an Aperiodic Task Server
12:25	Manuel Gericota°, Gustavo Alves°, Luís Lemos°, José Ferreira²	°Dept. of Electrical Engineering -ISEP, Porto Portugal; ²Dept. of Electrical and Computer Eng. - FEUP, Porto, Portugal	A New Approach to Assess Defragmentation Strategies in Dynamically Reconfigurable FPGAs
12:40	Minoru Watanabe, Fuminori Kobayashi	Dept.of Systems Innovation and Informatics, Kyushu Institute of Technology, Japan	:A 1,632 gate-count zero-overhead Dynamic Optically Reconfigurable Gate Array VLSI

12:55	**LUNCH**		
14:15	**NETWORK AND TELECOMMUNICATION**	**SESSION CHAIR : LUIGI CARRO**	
14:15	Sanjay P Singh, S. Bhoj, D. Balasubramanian, T. Nagda, D. Bhatia, P. Balsara	Center for Integrated Circuits and Systems; University of Texas, USA	Generic Network Interface for Plug and Play NoC based Architecture
14:40	Nikolay Kavaldjiev, Gerard Smit, Pascal Wolkotte, P. Jansen	Faculty of Electrical Engineering, Mathematics and Computer Science, University of Twente, the Netherlands	Providing QoS Guarantees in a NoC by Virtual Channel Reservation
15:05	Milan Tichy°, Jan Schier², David Gregg°	°University of Dublin, Trinity College, Dept. of Computer Science, Dublin, Ireland; ²Institute of Information Theory and Automation, Academy of Sciences of the Czech Rep., Czech Republic	Efficient Floating-Point Implementation of High-Order (N)LMS Adaptive Filters in FPGA
15:20	HongzhiWang, Pierre Leray, Jacques Palicot	IETR/ Supelec – Campus de Rennes, France	A reconfigurable architecture for MIMO Square Root Decoder
15:35	**BREAK**		**POSTER**
15:55	**SECURITY**	**SESSION CHAIR : WALID NAJJAR**	
15:55	Nele Mentens, L. Batina, B. Preneel, I. Verbauwhede	Katholieke Universiteit Leuven, ESAT/SCD-COSIC; Belgium	Time-memory trade-off attack on FPGA platforms: UNIX password cracking
16:20	F.-X. Standaert, F. Mace, E. Peeters, J.-J. Quisquater	UCL Crypto Group; Belgium	Updates on the Security of FPGAs against Power Analysis Attacks
16:45	K. Sakiyama, N. Mentens, L. Batina, B. Preneel, I. Verbauwhede	Katholieke Universiteit Leuven, ESAT/COSIC; Belgium	Reconfigurable Modular Arithmetic Logic Unit for High-performance Public-key Cryptosystems
17:10	Maurice Keller, Tim Kerins, Francis Crowe, William Marnane	Dept. of Electrical and Electronic Engineering, University College Cork; Ireland	FPGA Implementation of a GF(2^m) Tate Pairing Architecture
17:35	Guerric Meurice de Dormale, Jean-Jacques Quisquater	Université Catholique de Louvain, UCL, Crypto Group, DICE; Belgium	Iterative Modular Division over GF(2^m): Novel Algorithm and Implementations on FPGA
18:00	David Rodríguez, Juan M. Sánchez, Arturo Durán	Area de Arquitectura y Tecnología de los Computadores Esuela Politécnica, Universidad de Extremadura; Spain	Mobile Fingerprint Identification using a Hardware Accelerated Biometric Service Provider
18:15	S. Yusuf, W. Luk, M. Szeto, W. Osborne	Dept. of Computing, Imperial College London, UK	UNITE: uniform hardware-based network intrusion detection engine
18:40	**CONFERENCE DINNER**		

FRIDAY MARCH 3, 2006			
	TOOLS	**SESSION CHAIR : GEORGI KUZMANOV**	
09:30	Betul Buyukkurt, Zhi Guo, Walid Najjar	Dept. of Computer Science and Engineering, University of California-Riverside; USA	Impact of Loop Unrolling on Area, Throughput and Clock Frequency in ROCCC: C to VHDL Compiler for FPGAs
09:55	Dinesh Suresh, Zhi Guo*, Betul Buyukkurt, Walid Najjar	Dept. of Computer Science and Engineering; *Dept. of Electrical Engineering, University of California-Riverside; USA	Automatic compilation framework for Bloom filter based intrusion detection
10:10	Jie Guo°, Gleb Belov², Gerhard Fettweis°	°Vodafone Chair Mobile Communication Systems – TU Dresden, Germany; ²Fak. Mathematics and Natural Sciences, T.U. Dresden, Germany	A Basic Data Routing Model for a Coarse-grain Reconfigurable Hardware
10:25	B. De Sutter°, B. Mei°, A. Bartic°, T. Vander Aa°, M. Berekovic°, J-Y Mignolet°, K. Croes°, P. Coene°, M. Cupac°, A. Couvreur°, A. Folens°, S. Dupont°, B. Van Thielen°, A. Kanstein², H-S. Kimⁿ, S.J. Kimⁿ	°IMEC; Belgium; ²Freescale Semiconducteurs France SAS, France; ⁿSamsung Advanced Inst. of Techn.	Hardware and tool chain implementation for a coarse-grained reconfigurable architecture
10:40	Jack Whitham, Neil Audsley	Dept. of Computer Science, University of York, York, UK	Integrating Custom Instruction Specifications into C Development Processes
11:05	**BREAK**		
11:25	Jens Braunes, Rainer G. Spallek	Institute of Computer Engineering, Technische Universität Dresden; Germany	A Compiler-Oriented Architecture Description for Reconfigurable Systems
11:40	Antonio Beck, Victor Gomes, Luigi Carro	Instituto de Informática – Universidade Federal do Rio Grande do Sul, Brazil	Dynamic Instruction Merging and a Reconfigurable Array: Dataflow Execution with Software Compatibility
11:55	Jae-Jin Lee, Gi-Yong Song	School of Electrical and Computer Eng., Chungbuk National University; Korea	High-Level Synthesis Using SPARK and Systolic Array
12:10	Jae-Jin Lee, Gi-Yong Song	School of Electrical and Computer Eng., Chungbuk National University; Korea	Super Semi-Systolic Array-based Application-Specific PLD Architecture
12:25	**CLOSING**	**STAMATIS VASSILIADIS**	
POSTERS	J. Gonzalez-Gomez, I. Gonzales, F. Gomez-Arribas, E. Boemo	Universidad Autonoma de Madrid, Spain	Evaluation of a locomotion algorithm for worm-like robots on FPGA-embedded processors
	Ignacio Bravo, Pedro Jimenez, Manuel Mazo, Jose Luis Lazaro, E	Electronics dept. University of Alcala, Spain	Architecture based on FPGA's for real-time image processing
	Yeong-Jae Oh, Hanho Lee, Chong-Ho Lee	School of Information and Communication Engineering, Inha University, Korea	Dynamic Partial Reconfigurable FIR Filter Design
	Rodrigo Agis, Javier Diaz, Eduardo Ros, Richard Carillo, Eva Or	University of Granada, Spain	Event-driven simulation engine for spiking neural networks on a chip
	Eva Ortigosa, A. Canas, R. Rodriguez, J. Diaz, S. Mota	University of Granada, Spain	Towards an optimal implementation of MLP in FPGA
	E. Ros, J. Diaz, F. Vargas-Martin, M.D. Pelaez-Coca	University of Granada, Spain	Real time image processing on a portable aid device for low vision patients.
	S. Mota, E. Ros, J. Diaz, F. de Toro	University of Cordoba, University of Granada, Spain	General purpose real-time image segmentation system
	Joon ho park, Bang-Hyun Sung, Seok-Yoon Kim	Soongsil University, Korea	An Efficient Estimation Method of Dynamic Power Dissipation on VLSI Interconnects